**(Tris) Jiayi Tian**

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**Education**

**Nanjing University Nanjing, China**

School of Electronic Science and Engineering Sept. 2019- Jul. 2023

* B.Eng., Major in VLSI Design & System Integration
* **Cumulative GPA: 4.51/5.0; Major GPA: 4.49/5.0 (Top 10% in the grade)**

**Awards**

* National Undergraduate Electronic Design Contest, The 2nd Prize in Jiangsu Province, Nov. 2021(30%)
* National Undergraduate Electronic Design Contest, The 2nd Prize in Jiangsu Province, Oct. 2020(30%)
* People's Scholarship, The 2nd Prize in NJU, Nov. 2020(10%)
* Jinxiao Company Scholarship, Nov. 2021(5%)
* People's Scholarship, The Academic Competition Award, Nov. 2021(5%)

**Research Experience**

**Low-bit Quantization Work of BERT in the NLP Area**

*Independent Project, Apr. 2021-Oct. 2022*

* Used Python and Pytorch to perform low-bit quantization in BERT models and enhance their efficiency and robustness.
* Investigate literature on Transformer-based models and learn about the model compression methods for BERT.
* Substitute the knowledge distillation methods with ensemble techniques and boost the efficiency and robustness of binary BERT.
* Give reports biweekly on the project progress at the group meeting in Professor Zhongfeng Wang's research group with his Ph.D. and master's students
* **Preparing for ICASSP23's submission recently**

**INT8 Quantization Work of BERT with Hardware Deployment**

*Member, Sept. 2021-Dec. 2022*

* Used Python and Pytorch to perform INT8 quantization in BERT models
* Used Matlab to achieve the BERT models' encoder layer for a better understanding of the attention mechanism
* Now, my team is trying to use Verilog to deploy the BERT models' inference process on Hardware
* Give team reports on the project progress in biweekly team meetings

**VLSI Design Experiment**

*Individual assignment, March. 2022~June. 2022*

* Used Vivado and Cadence to devise efficient coding for computing 1-dimension convolution
* Proposed three optimization methods based on basic VLSI techniques, including pipeline, parallel, and transpose
* Wrote a report in 11 pages by Latex and got an A score

**Verilog Design Experiment**

*Member, Mar. 2021-Jun. 2021*

* Used Quartus and Intel Cyclone5 Series' FPGA to complete a VGA display clock on the monitor, which can set time via keyboard
* Responsible for accomplishing the VGA display, mainly used RAM and sequential logic analysis for designing
* Wrote a report in 17 pages by Latex and got an A+ score

**Extra-Curricular Experience**

**Student Union in Sch of Elec Sci and Eng., Organization Department**

*Department Director, Sept. 2020 - Sept. 2021*

* In charge of 2020 summer social practice, won "Excellent Organization Award" (20%)
* Won the 2021 "Excellent Department Director" (15%)
* Organized school social practice, volunteer work, and extracurricular activities

**Volunteer work**

* Achieved the 2021 "Excellent Volunteer Prize" (<1%)
* Achieved the "Excellent Volunteer Prize" on the school's 120th anniversary (<1%)

**School Badminton Association, Activity Department**

*Vice-chairman, Sept. 2021-Sept. 2022; Minister, Sept. 2020- Sept. 2021*

Organized large-scale sports events and contests in NJU, the number of participants is up to hundreds

**Women's Volleyball Team**

*Captain, Sept.2021-Sept. 2022*

Won the 4th prize in the 2019-2020 departmental contest and the 3rd prize in the 2020-2021 departmental contest

**Technical Skills**

* Programming and HDL:

Advanced in C/Matlab, Proficient in Verilog, Python/Pytorch, Familiar with C++

* Hardware design and simulation skills:

Advanced in Vivado/Quartus/Modelsim, Altium Designer, and Multisim, Familiar with SPICE

* TOEFL 102; GRE 153+170